P A T E N T C L A I M S

1. Synchronization circuit for processing an external sequence of analog values which is derived from an input sequence, comprising an analog feedback shift register (1), in which analog values stored in memory locations of a shift register (6) are combined according to a specific feedback pattern for deriving a feedback value according to a feedback function, from which a new input value is generated by superposition with a new element of the external sequence, which input value is fed to the input of the shift register (6), **characterized in that** the feedback function is substantially a linear combination of the arguments within substantially each sector characterized by specific values of the signs of the arguments.

2. Synchronization circuit according to Claim 1, **characterized in that** the magnitude of the feedback function is 1 if the magnitudes of the arguments are each 1.

3. Synchronization circuit according to Claim 1 or 2, **characterized in that** the sign of the feedback function always corresponds to the sign of the combination of the arguments.

4. Synchronization circuit according to any of Claims 1 to 3, **characterized in that** the feedback function is invariant when the arguments are interchanged.

5. Synchronization circuit according to any of Claims 1 to 4, **characterized in that** the feedback function as a

function of each argument is antisymmetrical and monotonic.

6. Synchronization circuit according to Claim 1, **characterized in that** the magnitude of the feedback function substantially corresponds to the mean value of the magnitudes of the arguments.

7. Synchronization circuit according to any of Claims 1 to 6, **characterized in that** the feedback value is produced by multiplying the value of the feedback function by a factor $k<1$, which is preferably between 0.90 and 0.99.

8. Synchronization circuit according to any of Claims 1 to 7, **characterized in that** it comprises a feedback circuit (7) for evaluating the feedback function and a gain block (8) for multiplying its initial value with a factor and an adder (5) for superposing the feedback value with a new element of the external sequence.

9. Synchronization circuit according to Claim 8, **characterized in that** it comprises a discriminator (9) for generating a binary output signal indicating completed synchronization, the input of which is connected to the output of the feedback circuit (7) and which preferably comprises a squaring circuit or another circuit mapping an input signal into the positive domain, a low-pass filter and a threshold value detector.

10. Synchronization circuit according to any of Claims 1 to 9, **characterized in that** it has a buffer (2) in front of the analog feedback shift register (1) for adding successive segments of an input sequence, each of which

contains a fundamental sequence, for generating the external sequence.

11. Synchronization circuit according to Claim 10, **characterized in that** the buffer comprises a shift register (4) and an adder (3) in front of it for adding a member of the input sequence to an output value of the shift register (4).